TECHNICAL MANUAL

for

Model DMB 6400 Series
S-100 Dynamic Memory Module

Systems Group
A Division of MEASUREMENT systems & controls incorporated

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1.0 Memory Features

The memory board you have purchased from Measurement Systems & Controls is a state of the art product which incorporates features not normally found in similar memory products. The incorporation of these features has been the result of a thorough research of existing dynamic memories, as well as long and exhaustive conversations with dynamic memory users. We are very proud of the successful implementation of these ideas into our product, and firmly believe that these features differentiate us from the other memory board manufacturers. It is for this reason that they will be introduced and explained first, before the theory of operation of the board is attempted.

Memory Interface

The memory board interfaces to the CPU through a 100 line computer bus, the S-100 BUS. Not all 100 lines are used with the memory board, nor have all lines been defined by the CPU suppliers.

The memory board follows the conventions established by early S-100 BUS users, as well as the latest attempt by the IEEE to standardize the S-100 BUS.

The following lines interface to the memory.

* 16 Data Lines
* 16 Address Lines
* 6 Status Lines
* 8 Control Lines
* 2 Clock Lines

DATA LINES - There are two groups of 8 data lines. Eight data lines are the input to the processor (DIØ-DI7). Eight data lines are the output from the processor (DOØ-DO7).

ADDRESS LINES - Sixteen address lines are used to identify a particular address location within the memory. Sixteen lines are sufficient to address 65,536 locations in memory. Each location can store 8 bits of information, one BYTE. The memory board can store 65,536 bytes of information in its fully implemented version (DMB6400).

STATUS LINES - The memory board utilizes the following Status Lines from the CPU board or from the Monitor Board.

* SMEMR (Memory Read)
* SM1 (M1 Status Line)
* SINTA (Interrupt Acknowledge)
* SINP (Input Operation from a peripheral, other than memory)
* SOUT (Output Operation to a peripheral, other than memory)
* $\overline{SWO}$ (Write Operation)

These signals are used to either control the operation of the memory or to disable it during the times when the memory is not being used as part of a machine cyle. The utilization of these lines by the memory board will be defined later in other sections of this technical manual.

CONTROL LINES - The memory board utilizes the following control lines.

* $\overline{\text{PWR}}$ (Processor Write)
* PDBIN (Processor Data Bus In)
* PSYNC (Processor Sync Pulse)
* PWAIT (Processor Wait)
* $\overline{\text{PHANTOM}}$ (Memory Disable)
* $\overline{\text{PRESET}}$ (Processor Reset)
* PRDY (Processor Ready Line)
* XRDY (Processor Ready Line)

These lines are used to start the read and write cycles of the memory. They are also used to make the processor wait for memory when operating with a floppy disc. Their full characterization and interfacing to the memory will be given later.

CLOCK LINE - The 8080 and Alpha Micro CPU's require the use of either $\emptyset_2$ or $\emptyset_1$, respectively, to determine the proper time for a refresh cycle. The correct clock line is switch selectable. Z80 CPU's do not require either clock signal as refresh is started after the falling edge of SM1.

Signal Buffering

The DMB6400 series memory boards use RC filters and buffers on the address and critical control lines. The purpose of the RC filters is to guarantee compatible operation of the memory board with 4 MHz CPU's on long, unterminated S-100 busses. The filters prevent false addressing and false memory timing on a long bus that characteristically exhibits voltage spikes and ringing.

The low power Schottky (LS) buffers minimize loading of bus source drivers and provide additional noise immunity by the use of Schmitt trigger devices. The input filters and LS buffers are compatible with both terminated and unterminated busses.

BANK SELECT

The Bank Select features incorporated in the DMB6400 series allows the user to do Multi-Tasking and Multi-User operations. Four independent 16K byte bank selectable sections give the user total freedom in determining their configuration. For example, the four bank selectable sections can reside at different address spaces and can all be turned on or off together to act like a single 64K byte bank of memory. Or each of the four bank selectable sections can reside at the same address space such

that there are 4 different banks of 16K bytes each. Any configuration between these two extreme cases can also be set-up such as two banks of 32K, one bank of 16K and one bank of 48K or a non bank selectable portion of memory of any multiple of 16K with the remaining memory selectable as one or more banks.

An eight section dip switch allows any one of the possible 256 I/O addresses to be decoded for turning on or off the banks. A second eight section dip switch controls the starting address for each of the four bank selectable sections. Each section can have a starting address of 0000H, 4000H, 8000H, or C000H. A four section switch determines which sections will be turned on or off during a system reset operation. An eighteen pin header gives total freedom in determining which of the eight data out lines will be used to turn on or off a bank in addition to making the bank select logic compatible with either the Cromemco/Alpha Micro or North Star methods for bank selection.

In addition there are four LED's in the upper left hand corner corresponding to bank one on the left and bank four on the right. Whenever a bank selectable section is on, its corresponding LED will be on. This is a very useful feature for doing software diagnostics on the memory board.

There are also times when it is desirable to deselect the entire memory in order to prevent it from writing on the BUS. The following cases are of interest:

* During a Power ON reset
* During a Reset cycle
* During an INPUT operation
* During an OUTPUT operation
* During an INTERRUPT ACKNOWLEDGED operation

System Reset and Extended Wait States

It is imperative that dynamic memory devices be refreshed often enough to retain their data. Two cases where refresh is critical are during system reset and extended wait states.

System reset is initiated by depressing the reset button. This grounds BUS pin 75 ($\overline{\text{PRESET}}$), causing all CPU operations to cease. When this occurs, a latch on the memory board is set which disables reads or writes and enables internal refresh.

An extended wait state is caused when a memory or I/O asserts the PRDY or XRDY lines to the processor. The processor in turn generates PWAIT, indicating that the processor is waiting for the memory or I/O device to complete its function. This only becomes a refresh problem when the wait state extends for several microseconds, such as occurs with some types of floppy disk controllers. The PWAIT or PRDY or XRDY signal is received from the bus and is internally delayed by 5, Ø2 clocks. After this delay, the logic compares this count with PRDY, XRDY or the reset

latch and enables refresh until PRDY and XRDY are reset and the reset latch is cleared. The reset latch is cleared by the first normal refresh generated after the processor starts up again. This assumes that the first instruction after a reset will not come from the dynamic RAM board.

Phantom Line Operation

After a power ON or system reset, it is usually desirable to have a monitor board or bootstrap ROM take control of the system operation. However, most CPU's will commence execution at location 0000H, an address usually recognized by the memory board. One way to avoid conflict between the memory board and the monitor or ROM is to set BUS pin 67, the $\overline{\text{PHANTOM}}$ line, to a low condition. When this line is low, the output buffers to the DI bus are disabled, and any write from memory operations are inhibited. This allows the CPU to jump to the monitor address space. In some cases a program may be executed out of ROM causing the $\overline{\text{PHANTOM}}$ line to be low until this program is completed. A four section dip switch allows each of the four bank selectable sections to individually select whether or not they are connected to the $\overline{\text{PHANTOM}}$ line. In those cases where the PHANTOM line is not used, all four switches should be in the off position.

I/O and Interrupt Mode Selection

During I/O and Interrupt Acknowledge cycle, it is necessary to disable the output buffer of the memory board. However, the memory board will continue to execute refreshes.

When any of these inputs are asserted, the SEL (select) signal will go low. The absence of board select disables the output buffers to the DI bus.

SINTA (BUS pin 96) is also received and is used to disable board select. If BUS pin 96 does not function for interrupts in your system, cut the etch at jumper area A and wire pad 2 to pad 3, disabling this signal.

DMA Compatibility

DMA operations involve an exchange of bus control between the processor card and an I/O device. The processor responds by raising pin 26 (PHLDA) granting control to the I/O device. The I/O device must then assert the necessary processor signals while removing the corresponding processor outputs from the bus. This will generally involve pulling low, BUS pins 19 ($\overline{\text{CCDSBL}}$), 22 ($\overline{\text{ADDR DSBL}}$), and 23 ($\overline{\text{DODSBL}}$). BUS pin 18 ($\overline{\text{STAT DSBL}}$) will generally not be pulled low by any but the most complex DMA controllers, as these signals are not required to control memory operations.

Whatever signals are disabled from the processor must be enabled from the DMA controller. It is important to the memory board that the minimum amount of bus noise be generated by this exchange. The best way is for the DMA controller to execute the following sequence of operations when PHLDA is received:

1. Assert all signals to be disabled to their inactive state.

2. Pull the appropriate disable signals to remove the processor from the bus.

3. Generate the appropriate signals to perform the memory cycles necessary.

4. Raise the disable signals.

5. Remove all outputs being generated by the DMA board, including PHOLD.

The timing signals necessary to drive the memory board are minimal.

For memory reads, a PSYNC is required if the memory board is set up for an 8080 processor; in this case the PSYNC causes the read operation. For memory read with a Z80 processor, the operation is initiated by RDEN which will be jumpered to either SMEMR or PDBIN, according to the kind of Z80 processor being used. The data read will appear on the DI bus so long as RDEN is asserted and the board is otherwise selected.

For an 8080, refresh is enabled on each PDBIN ANDed with Ø2. For Z80's, refresh is enabled after each M1 read. The refresh oscillator is designed to refresh more often than necessary (91 KHz actual versus 64 KHz required) in order to allow some refreshes to be skipped. However, skipping too many in any one 2 ms period can potentially cause loss of data.

2.0 Memory Board Set Up

Before the memory board can be made operational, 2 headers must be wired and 5 switches correctly set. In a few instances the PC board jumper areas may need to be reconfigured. A description of each follows. Refer to the memory board layout in the appendix for the locations of each header and switch.

Header No. 1

Header No. 1 allows the user to customize the timing of the control logic to interface with as many S-100 CPU's as possible. Table 1 is a list of the control signals which are connectd on Header No. 1. Table 2 is a wiring list for Header No. 1 for various types of CPU's running at either 2, 3, or 4 MHz. The majority of the available CPU types are listed in Table 2. However, in the event that you may own one that is not listed, a description of the various header selections, in conjunction with the theory of operation and timing diagrams will allow you to correctly wire the headers.

A description of the header selections is as follows:

1. RDEN to SMEMR or PDBIN

   The read enable signal (RDEN) is used to enable the tri-state output buffer, U61, and in the case of the Z80, it is used to start a memory M2-M5 read cycle. For all 8080, 8085, and Alpha Micro CPU boards, PDBIN is the correct timing signal. For Z80 CPU's either SMEMR or PDBIN is used, depending on the particular CPU design. Whichever of the two signals uses the Z80 $\overline{RD}$ output signal directly or through some combinational logic (no one shots) is the correct signal to use.

2. DYIN to PSYNC or SM1

   The delay input (DYIN) signal is used to generate either $\overline{DY50}$ for Z80 CPU boards or $\overline{DY150}$ for 8080 and Alpha Micro CPU boards. For Z80 CPU boards, SM1 is used and for 8080 and Alpha Micro CPU boards, PSYNC is used.

3. START 1 to $\overline{DY50}$, $\overline{PSYRD}$, or PU

   START 1 is used to initiate a memory read cycle. In the case of the 8080 and Alpha Micro, PSYRD is connected to START 1. For all Z80 CPU boards, the M1 read cycle is started by using DY50. The 8085 does not use START 1 and connects it to PU.

4. START 2 to $\overline{\text{RDENB}}$ or PU

   The START 2 signal is connected to $\overline{\text{RDENB}}$ for all Z80 and 8085 CPU's and is used to start a memory read cycle. For the Z80, this is a M2-M5 read cycle. This signal is not needed for 8080 and Alpha Micro CPU boards. For this case START 2 connects to PU.

5. REFEN to $\overline{\text{DY50}}$, 8080REF or $\overline{\text{RDENB}}$

   Refresh enable (REFEN) determines when in time a refresh cycle is to be initiated. For Z80 CPU's, $\overline{\text{DY50}}$ (with DYIN connected to SM1) is used and for all 8080 and Alpha Micro CPU boards, 8080REF is used. The 8085 CPU board requires $\overline{\text{RDENB}}$ to be connected to REFEN.

HEADER NO. 1 SIGNAL NAMES

Pin	Signal Name
1	SM1
2	PSYNC
3	SMEMR
4	PDBIN
5	8080REF
6	PU
7	REFEN
8	$\overline{\text{RDENB}}$
9	RDEN
10	START 2
11	START 1
12	$\overline{\text{PSYRD}}$
13	$\overline{\text{DY50}}$
14	No Connection
15	No Connection
16	$\overline{\text{DYIN}}$

TABLE 1

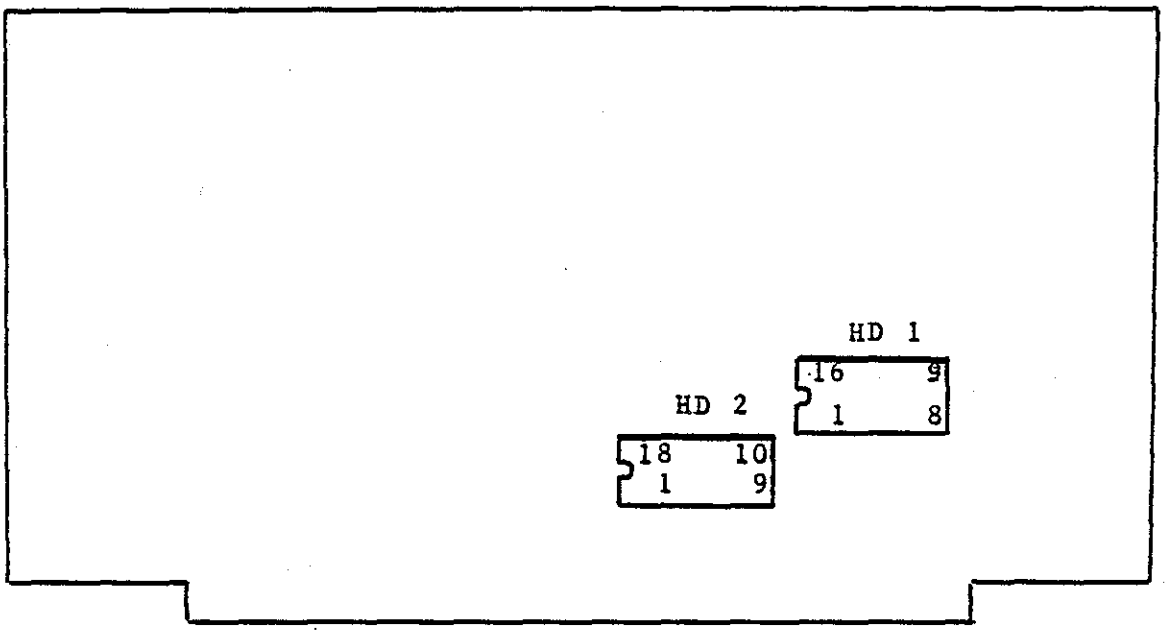


FIGURE 1

HEADER 1 & 2 PIN AND BOARD LOCATIONS

TOP VIEW

MEASUREMENT systems & controls incorporated	SHEET NO.	DWG. NO.	REV.
	9	TM DMB6400	B

HEADER NO. 1 WIRE LIST

CPU TYPE	HEADER NO. 1	
	Pin No. From - To	Function
8080 (All Types) Alpha Micro @ 2 MHz	2-16	(PSYNC = DYIN)
	4-9	(PDBIN = RDEN)
	12-11	($\overline{\text{PSYRD}}$ = START 1)
	6-10	(PU = START 2)
	5-7	(8080REF =REFEN)
SSM-CB2 Z80 Cromemco Z80 Delta Products Z80 GODBOUT Z80 North Star Z80 SBC-100/-200 TDL Z80 Vector Graphic Z80 @ 2 MHz or 4 MHz	1-16	(SM1 = DYIN)
	3-9	(SMEMR = RDEN)
	13-11	($\overline{\text{DY50}}$ = START 1)
	8-10	($\overline{\text{RDENB}}$ = START 2)
	13-7	($\overline{\text{DY50}}$ = REFEN)
Teletek Z80 Ithaca Audio Z80 @ 2 MHz or 4 MHz	1-16	(SM1 = DYIN)
	4-9	(PDBIN = RDEN)
	13-11	($\overline{\text{DY50}}$ = START 1)
	8-10	($\overline{\text{RDENB}}$ = START 2)
	13-7	($\overline{\text{DY50}}$ = REFEN)

TABLE 2

NOTE: ALL Header pins must be wired as described within each box for CPU types designated.

CPU TYPE	HEADER NO. 1	
	Pin No. From – To	Function
Space Byte 8085 *	4-9	(PDBIN = RDEN)
IMSAI 8085	6-11	(PU = START 1)
@ 3 MHz	8-10	($\overline{\text{RDENB}}$ = START 2)
*Disable SINTA as explained on sheet 17.	8-7	($\overline{\text{RDENB}}$ = REFEN)
Marin Chip M9900	1-16	(SMI = DYIN)
	3-9	(SMEMR = RDEN)
	6-11	(PU = START 1)
	8-10	($\overline{\text{RDENB}}$ = START 2)
	13-7	($\overline{\text{DY50}}$ = REFEN)

TABLE 2 (continued)

NOTE: ALL Header pins must be wired as described within each box for CPU types designated.

Header No. 2

Header No. 2 allows the user to configure the number and size of banks as well as which data out bits from the CPU will turn on or off each of the banks. (A logic 1 turns the corresponding bank on and a logic 0 turns it off.) In addition, either of two bank select methods (Alpha Micro/Cromemco or North Star) can be chosen by the wiring of Header No. 2. The Alpha Micro/Cromemco method will be described first.

The eight data out pins, DI0Ø - DI07 brought to Header No. 2 allow up to eight banks per I/O address to exist with a maximum of 4 banks per memory board. As many data out pins are used as there are banks per memory board. These data out pins are wired to the $J\overline{K}$Ø thru $J\overline{K}$3 signals which each represent one 16K bank selectable section. The DEØ thru DE3 signals are not used.

A single 64K byte memory board can be configured as 4-16K banks, 1-16K and 1-48K bank, 2-16K and 1-32K banks or 1-64K bank. Each 16K bank requires a single connection from one of the data out (DI0Ø - DI07) pins to one of the $J\overline{K}$ ($J\overline{K}$Ø - $J\overline{K}$3) pins. To configure a 32K bank two $J\overline{K}$ pins connect to the same data out pin. A 48K bank requires three $J\overline{K}$ pins to connect to the same data out pin and a 64K bank requires all four $J\overline{K}$ pins to connect to the same data out pin. The choice of which data out pin to use is determined by the software. Table 3 lists the signal names and pin numbers for Header No. 2.

The North Star bank select scheme is similar to the above description with the following differences. All four $J\overline{K}$ signals connect to DI0Ø and the DEØ thru DE3 signals take the place of the $J\overline{K}$Ø thru $J\overline{K}$3 signals, respectively. However only DI01 thru DI07 can now be used, limiting the user to a maximum of seven banks instead of eight.

In the case of the Alpha Micro/Cromemco bank select scheme, all banks can either be turned on or off with a single I/O output instruction. However, the North Star scheme requires two I/O output instructions to turn off or on all the banks--one instruction to turn off the banks and the second instruction to turn on the banks. This restriction is caused by connecting all four $J\overline{K}$ signals to DI0Ø which determines whether the banks addressed by DI00 thru DI07 are to be turned on or off.

If a particular block of memory is to be located in all banks, then wire PU (pullup) to the corresponding $J\overline{K}$ pins on Header No. 2. To keep a particular block of memory off all the time wire GND to the $J\overline{K}$ pins.

If the bank select feature is not used, then Header No. 2 does not need to be wired. (See the Application Note Section.)

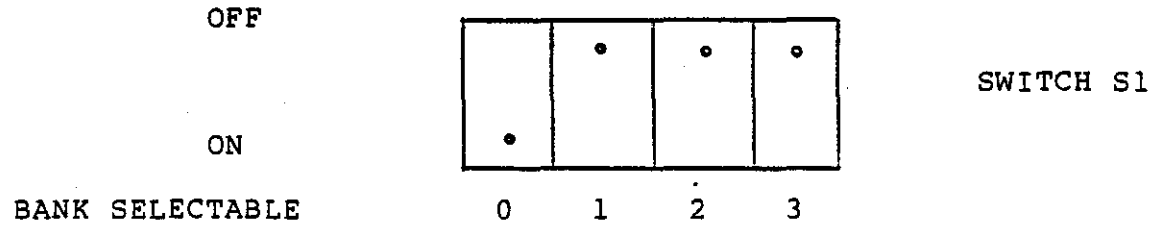
HEADER NO. 2 SIGNAL NAMES

Pin	Signal Name
1	DIOØ
2	DIO1
3	DIO2
4	DIO3
5	DIO4
6	DIO5
7	DIO6
8	DIO7
9	PU
10	GND
11	$\overline{JK}$3
12	DE3
13	$\overline{JK}$2
14	DE2
15	$\overline{JK}$1
16	DE1
17	$\overline{JK}$Ø
18	DEØ

TABLE 3

Switch S1

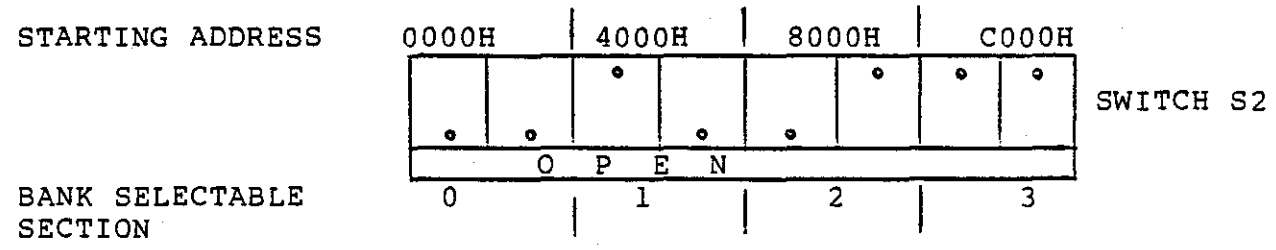
Switch S1 determines which bank selectable sections are turned on or off at system reset. It is a 4 Section SPDT switch which connects either the set or clear lines of the bank select flip flops (U42 & U37) to the RESET signal. The following diagram shows how to set this switch for bank selectable Section 0 on and 1-3 off.



Banks greater than 16K require all bank selectable sections that form the bank to be set to the same position, whether it be on or off. If the bank select feature is not used, all four bank selectable sections should be turned on at RESET for a 64K byte memory. If it is desired to deselect 16K of memory, then turn that section OFF at RESET.

Switch S2

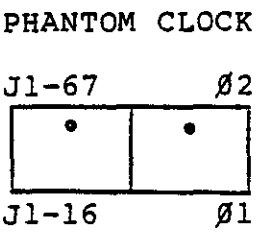
Switch S2 determines the starting address for each of the four 16K bank selectable sections. The eight section SPST switch uses 2 sections to generate the starting addresses of 0000H, 4000H, 8000H, and C000H. The 4 groups of 2 sections are selected the same way. The following diagram shows the location of each bank selectable section with each section set to a different starting address.



If the bank select feature is not used, then the four starting addresses should be set as pictured for a 64K byte memory configuration.

Switch S3

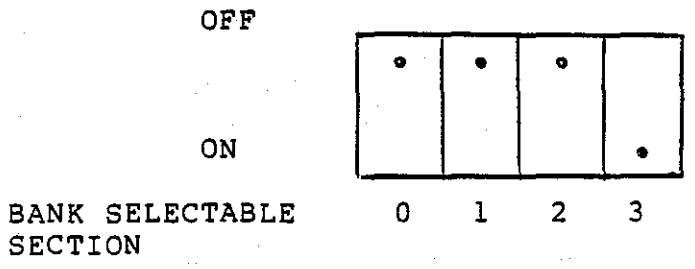
Switch S3 consists of two sections. The first one allows $\overline{\text{PHANTOM}}$ to connect to either J1-67 or J1-16 on the S-100 bus. Most systems generate $\overline{\text{PHANTOM}}$ on J1-67. However, the IMSAI MPU-B (8085) CPU board in particular generates $\overline{\text{PHANTOM}}$ on J1-16. The second section selects between Ø1 and Ø2 for the proper refresh timing. The Alpha Micro CPU requires Ø1 while all other CPU boards require Ø2. The following diagram shows the switches with PHANTOM in the J1-67 position and the clock in the Ø2 position.



SWITCH S3

Switch S4

Switch S4 determines which of the four bank selectable sections are connected to the $\overline{\text{PHANTOM}}$ signal. Thus any or all of the four bank selectable sections can be disabled whenever $\overline{\text{PHANTOM}}$ goes to a logic 0. The following diagram shows the settings for this switch with only bank selectable Section 3 connected to $\overline{\text{PHANTOM}}$.

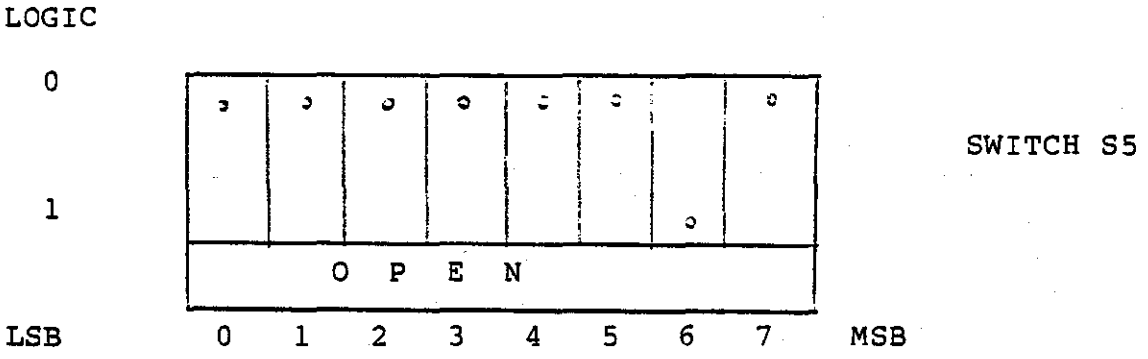


SWITCH S4

Switch S5

Switch S5 determines the 8 bit I/O address that the bank select circuitry will respond to. It is an 8 section SPST switch allowing 1 out of 256 possible addresses to be decoded depending on its switch setting. The following diagram shows the bit position locations with the address 40H set.

ADDRESS 40H SHOWN



If the bank select feature is not used, then set Switch S5 to an unused I/O address. If this is not possible, then wire JK̄Ø thru JK̄3 on Header No. 2 to the PU pin for an ON section and to GND for an OFF section.

PC Board Jumper Selection Areas

A: SINTA Enable/Disable

The memory board is delivered with SINTA enabled (pad 1 connected to 2) and allows a CPU generated SINTA signal to deselect the memory board. This is accomplished by causing the output data buffer to go to the tri-state condition. To prevent the SINTA signal from deselecting the memory board, the etch on the rear of the PC board between pads 1 and 2 must be cut and a wire added between pads 2 and 3.

B: PHANTOM Pullup Resistor

It is necessary that the PHANTOM line be pulled to +5 volts through a resistor. If this is not done on the CPU or some other board, then connect the pads in jumper area B together.

C: PWAIT ENABLE

Whenever an 8080 CPU board is used, the etch between pads 5 and 6 should be cut and a wire added between pads 4 and 5. This will allow the memory board to execute its refresh cycle during an 8080 HALT instruction.

(Jumper area C exists only on printed circuit boards labeled revision B and higher. On revision A boards, remove the wire from U58-1 to GROUND; located on the rear of the printed circuit board. Add a wire from U58-1 to the feed through immediately below this pin on the rear of the board.)

3.0 Theory of Operation

The design of the memory board is centered around the 4116 dynamic RAM chip, organized as 16K x 1 bit. Thirty-two of these devices are required for a 64K x 8 bit memory array and are arranged as four rows of 16K x 8 bits. The lower 14 bits (A0-A13) of the 16 bit address are used to directly address each of the four rows of memory and the highest 2 address bits (A14, A15) are decoded to determine which of the four rows is actually being accessed.

The 4116 has seven address inputs and requires a multiplexer to decode all 14 address inputs. The $\overline{RAS}$ and $\overline{CAS}$ inputs to the 4116 are used to multiplex the row and column addresses, each seven bits long, into the 4116 to construct a 14 bit address. The $\overline{WR}$ input determines whether the RAM is being read from ($\overline{WR}$ is logic 1) or written into ($\overline{WR}$ is logic Ø).

Data being read by the CPU is available from the 4116 on its Data out (DO) line and is latched into U61 (LS373), a tri-state device, at the appropriate time. U61 is enabled onto the S-100 bus by the ANDing of the read signal (either PDBIN or SMEMR, depending on the particular CPU board used) and SEL. SEL is generated whenever the memory board is selected.

Data to be written into memory is buffered by U60 (LS244), a line receiver and connects directly to the 4116 data in (DI) input.

The memory circuit contains three distinct timing cycles--memory read, memory write and memory refresh. The first two cycles require the 16 bit address from the S-100 bus while the refresh cycle uses an internally generated 7 bit counter address which refreshes each memory location in succession. U48 (MC3242A) performs the $\overline{RAS}$ and $\overline{CAS}$ address multiplexing previously discussed and also contains the refresh counter. During the read or write cycle, the REFEN input to U48 is a logic 0 and the seven address output lines (MA0-MA6) contain either the row (lower 7 address lines) or column (upper 7 address lines) address for the 4116 depending upon the state of the ROWEN input to U48. When REFEN is a logic 1, MA0-MA6 are the output of a seven bit counter which contains the refresh address. (Only seven address bits are needed for refresh corresponding to the 128 rows of memory internal to the 4116. Each time a single row is addressed, an entire column corresponding to 128 bits is refreshed.)

The $\overline{RAS}$, $\overline{CAS}$, and $\overline{WR}$ signals necessary for the 4116 as well as REFEN and ROWEN are generated by U36 (MC3480). U36 in turn requires a set of timing pulses, generated by delay lines U35 and U34. A description of this timing follows for the three different memory cycles. The actual details of the three memory cycles vary slightly depending on the type of CPU board used. All 8080 CPU boards function the same. However, depending on the particular Z80 CPU board used, the timing will vary slightly. Refer to the appropriate timing diagram.

Read Cycle

A read cycle is initiated by the rising edge of PSYNC (delayed by 150 ns) for the Alpha Micro and 8080 CPU's and either the rising edge of SM1 (delayed by 50 ns) for a Z80 M1 cycle or RDEN (PDBIN or SMEMR) for a Z80 M2-M5 cycle. U47B, U39A, U35, U41A, U40A, and U40D generate a pulse of approximately 100ns width that propagates through delay lines U35 and U34. The rising edges of the delay line outputs occur at 40 nanoseconds increments and are used as precision timing signals for the memory circuits. Forty nanoseconds after the start of a memory read cycle, T1 (U35-12) goes to a logic 1. T1 is an input to U36 and sets one of the four $\overline{RAS}$ lines to a logic 0 depending on address bits A14 and A15. (These two address lines are decoded by U36 into one of the four $\overline{RAS}$ outputs.) The falling edge of $\overline{RAS}$ latches the row address into the appropriate RAMs. Forty nanoseconds later T2 (U35-4) goes to a logic 1. ROWEN (U36-9) goes to a logic 0 causing U48 to output the column address. T3 (U35-10) goes to a logic 1 forty nanoseconds later, setting $\overline{CAS}$ to a logic 0. This latches the column address into the RAMs. During a read operation, the R/$\overline{W}$ input to U36 is a logic one. REFENB and R/$\overline{WR}$ are also a logic 1, causing T5 (U44B-6) to equal †8. When $\overline{†8}$ (U34-10) goes to a logic 1, U36 resets itself, with $\overline{RAS}$ and $\overline{CAS}$ going to a logic 1.

Approximately 100 nanoseconds after $\overline{CAS}$ goes to a logic 0, valid data appears at the output of the RAMs. OBCK (U51C-8) generated by the ANDing of $\overline{CAS}$ and RD†8 enables this data into output data buffer U61. Whenever RDOE (U38B-6) is a logic 0, this data is put on the S-100 bus by enabling the Tri-State output of U61.

Write Cycle

The write cycle is very similar to the read cycle just described. PWRB is NANDed with SEL to initiate a memory write operation. $\overline{RAS}$, the addresses and $\overline{CAS}$ are generated as during a read cycle. At T2 time, $\overline{SMWRITE}$ (U44A-3) is a logic zero, causing R/$\overline{WR}$ (U36-10) to go to a logic 0. T5 is equal to †6, causing U36 to be reset at †6 time instead of †8 time.

In the case of the Alpha Micro and 8080 CPU's, delayed PSYNC is ANDed with $\overline{SWO}$. $\overline{SWO}$ is the write status signal and is a logic 0 during a CPU write operation. Thus the delayed PSYNC signal is blanked out during a write cycle and is only used to start a memory read operation.

Refresh Cycle

The refresh cycle is performed transparently to all CPU's by executing the refresh operation during an unused time in the CPU timing cycle. For all Z80 CPU's this occurs after the trailing edge of SM1 and for all 8080 CPU boards this occurs after the

leading edge of the ANDing of PDBIN and $\overline{\emptyset_2}$. For the Alpha Micro CPU, refresh occurs after the leading edge of the ANDing of PDBIN and $\emptyset_1$. Once the refresh cycle is started it is identical for all CPU boards.

Refresh must occur for all 128 rows of each RAM within 2 milliseconds if all data is to be retained. Thus one of the 128 rows must have a refresh memory cycle performed at least every 15.6 usec. The free running oscillator, U56, runs at a frequency of 91 KHz and causes a refresh cycle to occur approximately every 11 usec. When REFCLK (U56-3) goes to a logic 1, it signals U36 that a refresh operation needs to occur. U36 responds by making $\overline{\text{RREQ}}$ (U36-20) a logic 0. This signal is inverted and delayed by U41,F,E&D and enables U52D.

The rising edge of REFEN (HD#1-7) triggers the one sot consisting of U54B, Q2 and U54A, generating a 60 nanosecond logic 0 pulse. If $\overline{\text{PRESET}}$ and PWAIT are not asserted, then $\overline{\text{REFENA}}$ (U54A-2) causes a refresh cycle to start. The falling edge of U52D-11 latches the J-K flip flop, U47A, generating a logic 1 (REFG) at its Q output. REFG (refresh grant) signals U36 to generate a refresh cycle when T1, T2, T3, etc. are generated. The REFEN output of U36 also enables the refresh counter in U48 to increment by one count. $\overline{\text{REFG}}$ (U39B-6) causes START (U39A-3) to go to a logic 1 which begins the generation of T1, T2, T3....., as for a write cycle. However, U36 is set for a refresh operation and causes all four $\overline{\text{RAS}}$ outputs to go to a logic 0. $\overline{\text{CAS}}$ and R/$\overline{\text{WR}}$ are not generated and as a result a single row of 128 bits in all 32 RAMs is refreshed. When †6 occurs, U36 is reset and is ready for the beginning of another memory cycle.

Bank Select

The memory array is configured as four independent bank selectable sections, 16K bytes each. At system reset time, $\overline{\text{RESET}}$ goes to a logic 0 and depending on the settings of Switch S1, J-$\overline{\text{K}}$ flip flops U42 and U37 are either set or cleared. Each flip flop that is set represents a bank selectable section that is turned on with its corresponding LED lit.

After this initialization, each of the banks can be turned on or off under software control. Whenever an I/O output instruction is executed, SOUT and PWRB are logic ones. U52B NANDs these two signals and enables the eight bit comparator, U59. If the lower eight address lines match the settings of Switch S5, then EOUT of U59 goes to a logic 0, triggering the one shot consisting of U52C and Q_1. The falling edge of this 60 nanosecond pulse clocks J-K flip flops U42 and U37, allowing enough time for DI0Ø thru DI07 to set up.

Header 2 gives the user the flexibility to utilize either of the two most common bank select methods. For the Cromemco and Alpha Micro bank select operations, any of the eight data lines, DIØØ thru DI07 can be wired to the four J-K inputs on flip flops U42 and U37. This allows any combination of the eight data lines to turn on or off any or all of the four bank selectable sections. Thus with one I/O command, the state of all banks can be changed and the banks can be configured to be any multiple of 16K bytes.

To be compatible with the North Star method, all four J-$\overline{K}$ inputs are wired to DIØØ. This data bit determines whether the addressed banks are to be turned on or off. The DI01 thru DI07 data bits are then wired to one of the four inputs of NAND gate U43 according to the users bank select requirements. In this scheme a single I/O command is necessary to turn on the banks and a second instruction is necessary to turn off the banks.

After a 16K bank selectable section of memory has been turned on, its location in the memory space is determined by the settings of Switch S2. Dual comparators U45 and U55 compare address bits A14 and A15 with these settings, allowing each section to be located in any one of four possible locations. These locations start at 0000H, 4000H, 8000H, or C000H. U62B and U62D encode the four outputs of both comparators and drive the A14 and A15 inputs of U36. U62C and U44F OR the four outputs of the comparators so as to enable BSEL whenever any one of the bank selectable sections is turned on.

In addition to the above features, $\overline{\text{PHANTOM}}$ can be enabled independently for each of the four sections. Switch S4 determines whether a particular bank will be disabled or not when PHANTOM goes low by driving the fourth input of comparators U45 and U55.

The memory board is also disabled from outputing data whenever SINTA, $\overline{\text{PRESET}}$, SOUT or SINP are active. U57B and U51A OR these signals together and set SEL to a logic 0 whenever one of these signals is asserted.

PRESET and Extended PWAIT Circuit

During a PRESET for a CPU reset operation or an extended PWAIT for a CPU controlled floppy disc data transfer the normal CPU timing comes to a halt. To insure that refresh will continue it is necessary to initiate a refresh cycle independently of the other S-100 bus timing signals normally used to determine the refresh timing. $\overline{\text{PRESET}}$, PWAIT, PRDY or XRDY are ORed by U57A and after a fixed time delay determined by shift register U46, enable NAND gate U52D. A refresh cycle will begin whenever $\overline{\text{RREQ}}$ (U36-20) goes to a logic 0. The start of a refresh cycle is completely determined by free running oscillator, U56. The delay

introduced by U46 is necessary to allow the memory circuits to complete any memory read or write cycle that may have started just prior to the occurrence of either PRESET PWAIT, PRDY or XRDY.

Control and Address Line Filters

RC input filters and low power schmit trigger buffers are used on the address and critical control lines to prevent voltage spikes and bus ringing from causing false timing signals to occur. The design of the input filters and buffers assure compatible operation on an S-100 bus that is either terminated or unterminated.

4.0 Warranty

All Products sold hereunder are warranted on a return-to-factory basis against defects in workmanship and material under normal and proper use for a period of one (1) year from the date of delivery.

As a condition of this warranty, Purchaser must (i) obtain a Repair Order Number and shipping instructions from Measurement Systems and Constrols, Inc., (ii) ship the Product, transportation prepaid, to the designated Measurement Systems and Controls, Inc. Repair Facility in the United States, and (iii) include with the returned Product a written description of the claimed defect. Transportation charges for the return of the Product to Purchaser within the contiguous forty-eight (48) United States, Alaska, Hawaii and the District of Columbia will be paid by Measurement Systems and Controls, Inc. For Products returned from all other locations, this warranty will be honored at the nearest Measurement Systems and Controls, Inc. Repair Facility in the United States but excludes all costs of transportation, customs clearance and any other related charges. If Measurement Systems and Controls, Inc. determines that the Product is not defective as herein defined, Purchaser shall pay Measurement Systems and Controls, Inc. all costs of handling and transportation and any repairs will be at the then prevailing Measurement Systems and Controls, Inc. repair rates.

Measurement Systems and Control's Inc. sole responsibility under the above Product warranties will be, at its option, to either repair or replace any component which fails during the period of the applicable warranty due to a defect in workmanship or material, provided Purchaser has promptly reported same to Measurement Systems and Controls, Inc. All replaced Products or parts shall become Measurement Systems and Control's, Inc. property.

All above warranties are contingent upon proper use of the Product. These warranties will not apply (i) if adjustment, repair or parts replacement is required because of accident, unusual physical, electrical or electro-magnetic stress, neglect, mis-use, failure of electric power, air conditioning, humidity control, transportation, failure of rotating media not furnished by Measurement Systems and Controls, Inc., operation with media not meeting or not maintained in accordance with Measurement Systems and Controls, Inc. specifications or causes other than ordinary use, or (ii) if the Product has been modified by Purchaser, or (iii) where Measurement Systems and Controls, Inc. serial numbers or warranty date decals have been removed or altered, or (iv) if the Product has been dismantled by Purchaser without the supervision of or prior written approval of Measurement Systems and Controls, Inc.

EXCEPT FOR THE EXPRESS WARRANTIES CONTAINED HEREIN, MEASUREMENT SYSTEMS AND CONTROLS, INC. DISCLAIMS ALL WARRANTIES ON THE PRODUCTS FURNISHED HEREUNDER, INCLUDING ALL IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS; and the stated express warranties are in lieu of all obligations or liabilities on the part of Measurement Systems and Controls, Inc. arising out of or in connection with the performance of the Products. Measurement Systems and Controls, Inc. is not liable for any indirect or consequential damages.

After the warranty period, the Products will be repaired for a service charge plus parts, provided that it is returned prepaid to Measurement Systems and Controls, Inc. after retaining a Repair Order Number.

PARTS LIST REVISION A

ITEM	DESCRIPTION		QTY	REMARKS
1	7400N	QUAD NAND GATE	3	U38,U43,U53
2	74S00N	QUAD NAND GATE	1	U44
3	7402N	QUAD NOR GATE	1	U62
4	74S04N	HEX INVERTER	1	U54
5	7408N	QUAD AND GATE	1	U40
6	74S11N	TRI AND GATE	1	U51
7	74LS13N	DUAL NAND GATE	1	U57
8	74LS14N	HEX INVERTER	3	U41,U58,U63
9	74LS109N	DUAL $J\overline{K}$ F/F	2	U37,U42
10	74S112N	DUAL JK F/F	1	U47
11	74LS132N	QUAD NAND GATE	2	U39,U52
12	74164N	SHIFT REGISTER	1	U46
13	74LS244N	OCTAL BUFFER	1	U60
14	74LS373N	OCTAL LATCH	1	U61
15	MC4022BCP	DUAL COMPARATOR	2	U45,U55
16	MC3242A	ADDRESS MUX	1	U48
17	MC3480L	RAM CONTROLLER	1	U36

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PARTS LIST

REVISION A

ITEM	DESCRIPTION		QTY	REMARKS
18	25LS2521	8 BIT COMPARATOR	1	U59
19	MK4116-3	16K DYNAMIC RAM	32	U1-U32
20	NE555	OSCILLATOR	1	U56
21	DDU-4-5200	DELAY LINE	2	U34,U35
22	DDU-4-5250	DELAY LINE	1	U64
23	2N2369A	TRANSISTOR	2	Q1,Q2
24	LM340T-5.0	VOLTAGE REGULATOR	1	VR1
25	LM340T-12	VOLTAGE REGULATOR	1	VR2
26	LM79L05ACZ	VOLTAGE REGULATOR	1	VR3
27	1N4001	DIODE	1	CR1
28	76B08	8-SPST SWITCH	2	S2,S5
29	76C04	4-SPDT SWITCH	2	S1,S4
30	76C02	2-SPDT SWITCH	1	S3
31	555-2007	LED (DIALIGHT)	4	CR2-CR5
32	4310R-101-103	SIP (BOURNS)	3	SIP1,SIP2,SIP4
33	4306R-101-103	SIP (BOURNS)	1	SIP3
34	22 ,5%, 1/8W	RESISTOR	13	R1-R13

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PARTS LIST REVISION A

ITEM	DESCRIPTION		QTY	REMARKS
35	68 ,5%, 1/4W	RESISTOR	1	R25
36	200 , 5%, 1/8W	RESISTOR	22	R18,R19,R21,R28-R46
37	RN55C4320F	RESISTOR, 1%	2	R17,R24
38	510 , 5%, 1/4W	RESISTOR	2	R16,R23
39	1K , 5%, 1/4W	RESISTOR	3	R14,R15,R22
40	9.1K , 5%, 1/4W	RESISTOR	1	R26
41	10K , 5%, 1/4W	RESISTOR	2	R20,R27
42	SR155A470MAA	47pf CAPACITOR	22	
43	CM05FD241J03	240pf CAPACITOR	2	C1,C2
44	CM05FD391J03	390pf CAPACITOR	1	C3
45	SR205E104ZAA	0.1uf CAPACITOR	123	
46	TANTALUM, 35V	6.8uf CAPACITOR	8	
47	308-AG39D	IC SOCKET	1	
48	314-AG39D	IC SOCKET	18	
49	316-AG39D	IC SOCKET	38	
50	318-AG39D	IC SOCKET	1	
51	ICN203SBG	IC SOCKET	3	

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ITEM	DESCRIPTION		QTY	REMARKS
52	324-AG39D	IC SOCKET	1	
53	328-AG39D	IC SOCKET	1	
54	616 CG1	COMPONENT ASSEMBLY	1	HD 1
55	618 CG1	COMPONENT ASSEMBLY	1	HD 2
56	HS371-220	HEAT SINK	2	AHAMTOR
57	DMB6400	PC BOARD	1	
58	6-32X3/8	SCREW	2	
59	6-32	NUT	2	
60	#6	LOCK WASHER	2	

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Application Note for Alpha Micro Users

1. Setup the first 64K memory board as follows for 32K user banks:

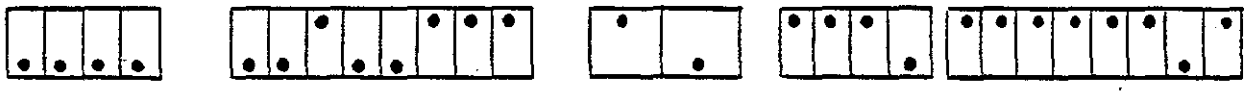
   A. Wire Header No. 2 as follows:
   - pin 1 to pin 17
   - pin 2 to pin 15
   - pin 3 to pin 13
   - pin 4 to pin 11

   B. See Technical manual, sheet 10 for Header No. 1.

   C. Use the following MEMDEF statement:

   ```
   MEMDEF 100, 17, 3
   ```

   D. Set Switches S1-S5 as follows:



2. Setup additional 64K memory boards to contain 2, 32K users banks each as follows:

   A. Wire Header No. 2 as follows:

   - pin 1 to pin 17
   - pin 2 to pin 15
   - pin 3 to pin 13
   - pin 4 to pin 11

   B. Use the following MEMDEF statements to create 4, 32K user banks:

```
MEMDEF      101,3,0             For Board 2
MEMDEF      101,14,0

MEMDEF      102,3,0             For Board 3
MEMDEF      102,14,0
```

   C. Set Switches S1-S5 as follows:

Board 2

Board 3

S5

S1 - S4 are the same as Board 2

3. The number of banks can be expanded by using more MEMDEF statements. Users banks of 16K may also be configured.

Application Note for Cromemco Systems

1. Setup the first 64K memory board as follows for 32K user banks for either single or multi-user systems:

   A. Wire Header No 2 as follows:

      - pin 1 to pins 15 and 17
      - pin 9 to pins 11 and 13

   B. See Technical Manual, sheet 10 for Header No. 1.

   C. Set Switches S1-S5 as follows:

2. Setup additional 64K memory boards to contain 2, 32K user banks each as follows for multi-user systems:

   A. Wire Header No. 2 as follows:

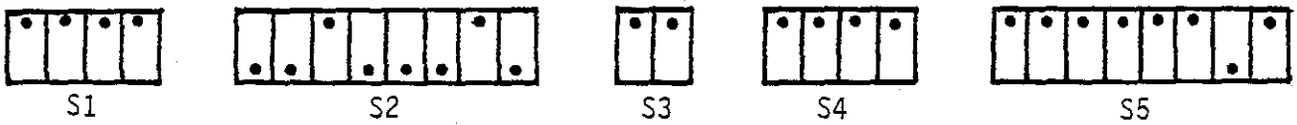
      - pin 2 to pins 15 and 17 — Board 2
      - pin 3 to pins 11 and 13

      - pin 4 to pins 15 and 17 — Board 3
      - pin 5 to pins 11 and 13

      - pin 6 to pins 15 and 17 — Board 4
      - pin 7 to pins 11 and 13

      - pin 8 to pins 15 and 17 — Board 5
        (Board 5 can be a DMB3200)

   B. Set Switches S1-S5 on all additional boards as follows:



3. Users banks of 16K may also be configured, requiring only 3 memory boards, where Board 3 can also be a DMB3200.

NOTE: See sheet A4 for Application Note for Cromemco Multi-user, CDOS, Rev. 1.50.

Application Note for Cromemco Multi-User, CDOS, REV 1.50

Note: The previous Cromemco Multi-User application note is for Multi-User CDOS, REV. 1.40

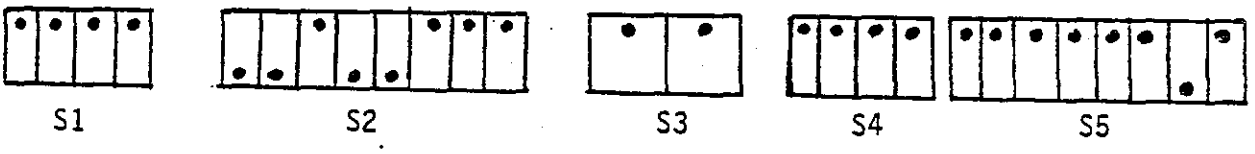
1. Setup the first 64K memory board as follows (2-32K banks):

   A. Wire Header No. 2 as follows:

      - pin 8 to pins 15 and 17
      - pin 9 to pins 11 and 13

   B. See Technical Manual, sheet 10 for Header No. 1.

   C. Set Switches S1-S5 as follows:

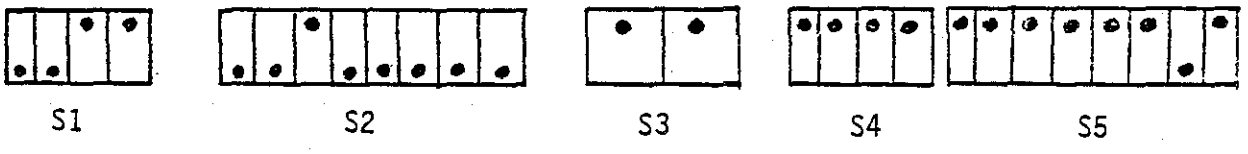


2. Setup the second 64K memory board as follows (1 user bank of 32K and 2 user banks of 16K):

   A. Wire Header No. 2 as follows:

      - pin 1 to pins 15 and 17
      - pin 2 to pin 13
      - pin 3 to pin 11

   B. Set switches S1-S5 as follows:

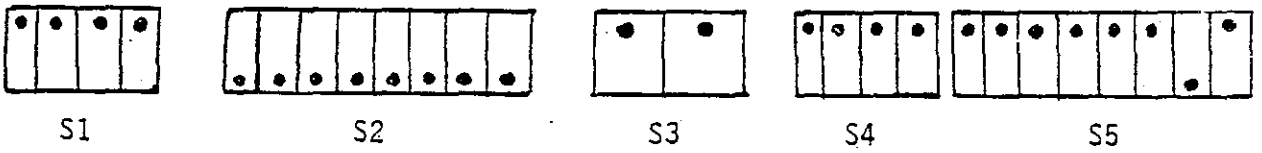


3. Setup the third 64K memory board as follows (4 user banks of 16K):

   A. Wire Header No. 2 as follows:

      - pin 4 to pin 17
      - pin 5 to pin 15
      - pin 6 to pin 13
      - pin 7 to pin 11

   B. Set switches S1-S5 as follows:



4. Note: User banks can be 32K instead of 16K. Refer to Section 2 of the manual for more details.

Application Note for Operation with Double Density Disc Controllers

Certain double density disc controllers such as Delta Products (when used with a non Delta Products CPU), Tarbell, IMS, Ithaca Intersystem, and Dynabyte, latch PHANTOM with a flip flop. This causes a race condition with the DMB6400 at boot up.

To correct this problem, set the starting address of bank 3 to ØØØØH.

In general, set the address of bank 3 to be in the same address space as the bootstrap ROM when PHANTOM is active.

Application Note for North Star Users

1. The early version of Micro Mikes multi-user software requires 32K banks of switchable memory starting from address 2000H. The DMB series of memory boards has switch selectable starting addresses of 000H, 4000H, 8000H and C000H. The following modification must be made to the DMB board to have two 32K banks of switchable memory from addresses 2000H to 9FFF H.

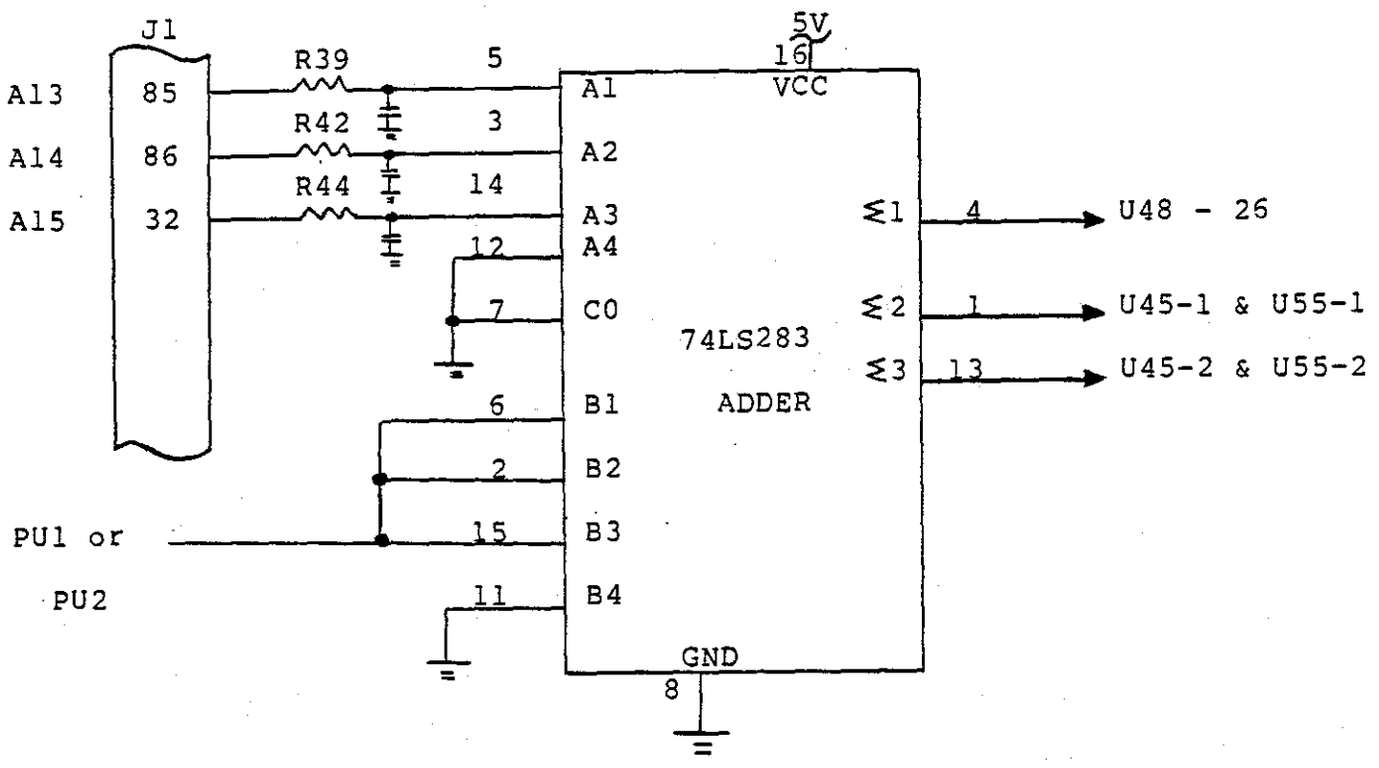
2. Add a 74LS283, 4 bit adder, to the empty IC location on the printed circuit board and make the appropriate etch cuts and wire additions to implement the following circuit. U63E and U63F are deleted as well as the connection from R39 to U48 pin 26.

   NOTE: Switch S2 positions are now opposite of the technical manual.

3. In addition, all four $J\overline{K}$ signals should be connected to $\overline{DIO\emptyset}$ and not $DIO\emptyset$ as described in the section discussing Header No. 2. To accomplish this, spare inverter gate, U63D, must be wired to Header No. 2 as follows:

   Wire U63D, pin 9 to HD2, pin 1
   Wire U63D, pin 8 to HD2, pin 17
   Wire HD2, pins 11, 13, 15, and 17 together, as before but do not wire these to HD2, pin 1.

4. Add 2000H to each of the addresses shown for switch S2 (sheet 14) to determine the new starting addresses for each bank.



CIRCUIT MODIFICATION FOR NORTH STAR USERS

Application Note for TEI 8085 @ 5 MHz

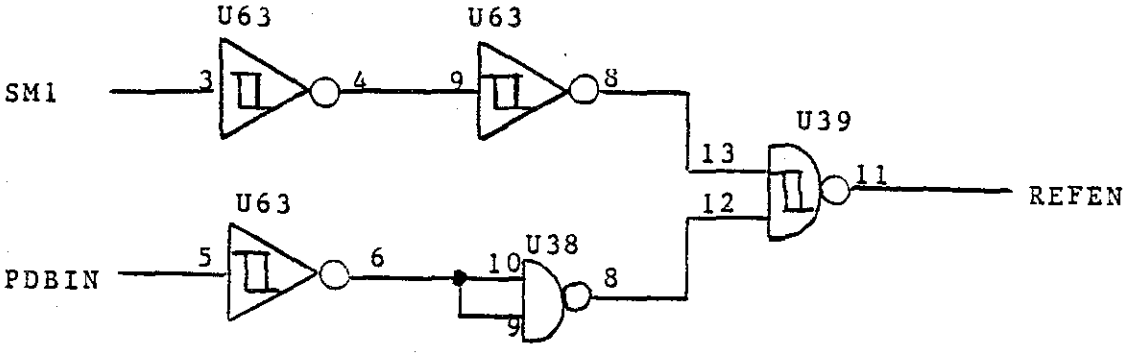
1. Add 1 wait state on CPU for all memory cycles.

2. Wire HD #1 as follows:

   - pin 4 to pin 9
   - pin 6 to pin 11
   - pin 8 to pin 10
   - pin 1 to pin 16

3. Add the following connections to generate REFRESH enable:

   - U63-4 to U63-9
   - U63-8 to U39-13
   - U38-8 to U39-12
   - U39-11 to U54-3



4. Make the following changes to enable auto refresh:

   - Cut J1-27 to jumper area C pad 4
   - Add wire from jumper area C pad 4 to J1-48
   - Cut jumper area C pads 5-6
   - Wire jumper area C pads 4-5

NOTE: The addition of the wait state is necessary for the DMB6400 to function correctly. However, the TEI double density controller card when used with 8" drives, requires that there be no wait states. Thus the DMB6400 is not recommended for this application. However, if a 5" drive is used or a non TEI double density controller is used, there will be no problems. The TEI controller in single density mode is also okay.

Application Note for Ithaca Intersystems IEEE CPU (Series II Z80 Processor)

The following modifications are required in order to interface the DMB6400 series memory boards to the Series II Z80 Processor:

1. The CPU must be operated in the unlatched mode by removing the JH-1 pin-jumper located on the right side of the processor board between U12 and U13.

2. Change the wiring for header number 1 to use SMEMR for RDEN instead of PDBIN as shown in Table 2 (wire pin 3 to pin 9).

Application Note to Deselect Memory

The following circuit modifications are required in order to deselect portions of memory.

General

The method described in this application note to deselect memory uses $\overline{\text{PHANTOM}}$ to disable the selected portions of memory. A logic gate is to be added to the spare location (U33) and then the required address bits are to be wired to the input of the logic gate. The output of the added gate then asserts the phantom signal in parallel with the system $\overline{\text{PHANTOM}}$ line whenever the wired address bits are a logic 1.

For systems that use $\overline{\text{PHANTOM}}$, an open collector logic gate is to be added (where an equivalent logic gate is available) in place of a device with an internal pullup. In addition, systems that use $\overline{\text{PHANTOM}}$ must also provide a 1K ohm pullup resistor somewhere in the system.

1. To deselect the upper 8K (E000-FFFF) of any bank, perform the following memory board modifications:

   A. Install a 74LS13 (or 74LS22 open collector gate) in position U33 on the memory board with pin 1 of the device located in the square hole of location U33.

   B. Add a wire from U33 pin 7 to U33 pin 8 (this wires a ground to the added gate).

   C. Add a wire from U33 pin 1 to pullup PPU (Resistor R14, 1K ohm).

   D. Add a wire from U63 pin 11 (74LS14) to U33 pin 2. (Address bit A15)

   E. Add a wire from U63 pin 13 (74LS14) to U33 pin 4. (Address bit A14)

   F. Add a wire from U48 pin 26 (MC3242) to U33 pin 5. (Address bit A13)

   G. Add a wire from U33 pin 6 to U41 pin 5 (74LS14). (Connects the new address decode circuit to the $\overline{\text{PHANTOM}}$ line.)

2. To deselect the upper 4K (F000-FFFF) of any bank, perform the following memory board modifications:

   A. Install a 74LS13 (or 74LS22 open collector gate) in position U33 on the memory board with pin 1 of the device located in the square hole of location U33.

   B. Add a wire from U33 pin 7 to U33 pin 8 (this wires a ground to the added gate).

   C. Add a wire from U63 pin 11 (74LS14) to U33 pin 1 (Address bit A15).

   D. Add a wire from U63 pin 13 (74LS14) to U33 pin 2 (Address bit A14).

E. Add a wire from U48 pin 26 (MC3242) to U33 pin 4 (Address bit A13).

F. Add a wire from U48 pin 24 to U33 pin 5 (Address bit A12).

G. Add a wire from U33 pin 6 to U41 pin 5 (74LS14) (connects the new address decode circuit to the PHANTOM line).

3. To deselect the upper 2K (F800-FFFF) or upper 1K (FC00-FFFF) of any bank, perform the following memory board modifications:

A. Install a 74LS30 (8 input NAND gate) in position U33 on the memory board with pin 1 of the device located in the square hole of location U33.

B. Add a wire from U33 pin 7 to U33 pin 8 (this wires a ground to the added gate).

C. Add a wire from U63 pin 11 (74LS14) to U33 pin 1 (Address bit A15).

D. Add a wire from U63 pin 13 (74LS14) to U33 pin 2 (Address bit A14).

E. Add a wire from U48 pin 26 (MC3242) to U33 pin 3 (Address bit A13).

F. Add a wire from U48 pin 24 (MC3242) to U33 pin 4 (Address bit A12).

G. Add a wire from U48 pin 22 (MC3242) to U33 pin 5 (Address bit A11).

H. Add a wire from U33 pin 8 to U41 pin 5 (74LS14) (connects the new address decode circuit to the PHANTOM line).

I. For the 2K DESELECT MODIFICATION ONLY perform this step. For the 1K deselect modification proceed to step J.

Add a wire from PPU (resistor R14, 1K ohm) to U33 pins 6, 11, and 12 (wires the unused inputs of U33 to a pullup).

J. FOR THE 1K DESELECT MODIFICATION ONLY perform this step:

Add a wire from U48 pin 20 (MC3242) to U33 pin 6 (Address bit A10).

Add a wire from PPU (resistor R14, 1K ohm) to U33 pins 11 and 12 (wires the unused inputs of U33 to a pullup).

Application Note for Non-Bank Select Users

If the bank select feature is not used, then Header number 2 does not need to be wired. However, to take maximum advantage of the noise rejection features it is recommended that the unused bank bit select lines be pulled up as follows:

For 64K boards:

On header number 2, wire: pin 9 to pins 11, 13, 15, and 17

For 32K boards:

On header number 2, wire: pin 9 to pins 15 and 17
pin 10 to pins 11 and 13

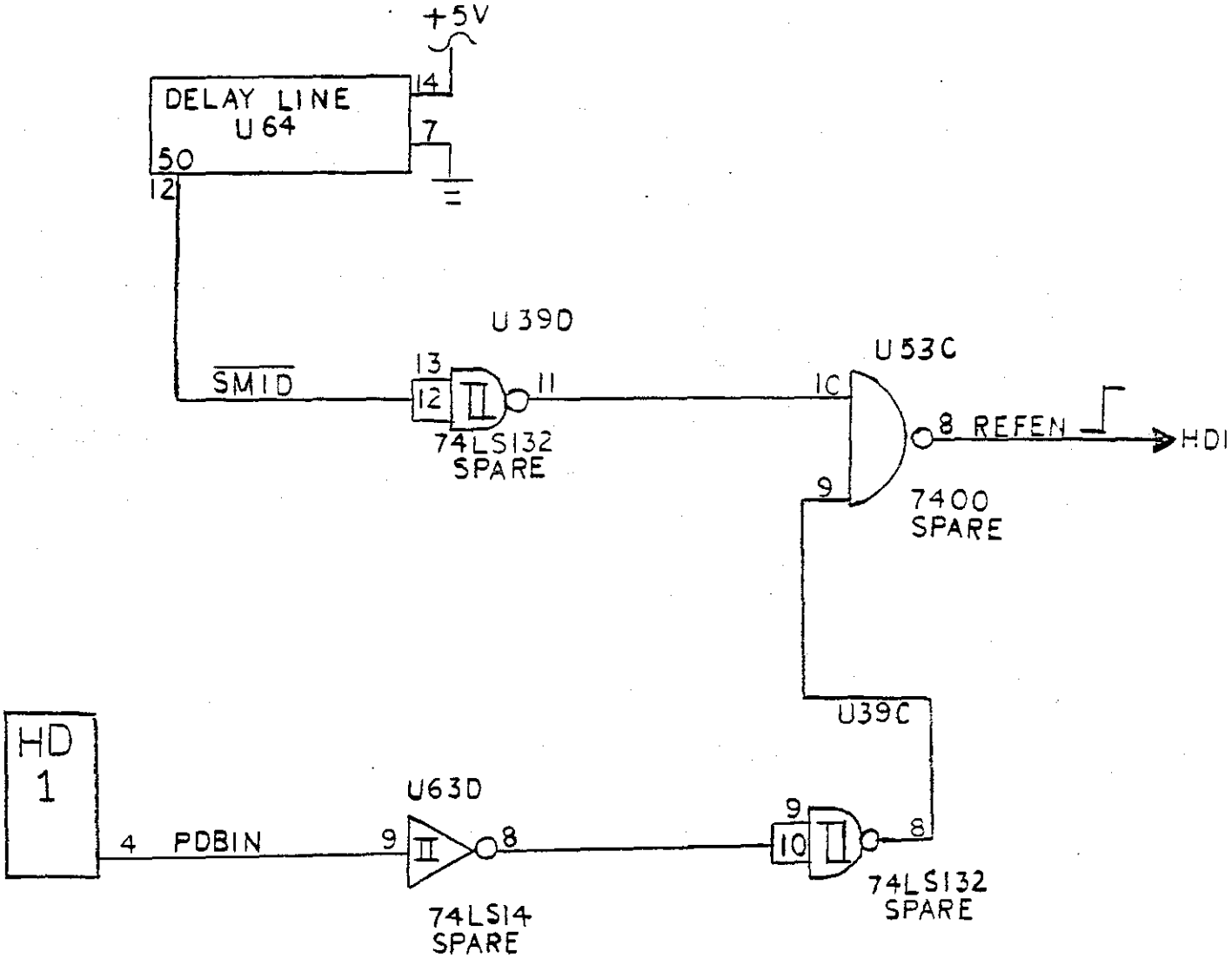
Application Note for IEEE Operation with the DMB6400

The DMB6400 can be modified to run with the newer CPU boards that meet the new proposed IEEE S-100 specification. The following changes will work with those CPU's that generate their status signals using a partial latch mode.

1. Add the following connections to generate REFRESH enable:

   U64-12 to U39-12 & 13
   U39-11 to U53-10
   HD1-4 to U63-9
   U63-8 to U39-9 & 10
   U39-8 to U53-9
   U53-8 to HD1-7

2. Wire Header No. 1 according to Table 2 for the appropriate Z80 CPU board, with one exception - do not connect anything to HD1-7.



Application Note for the Dynabyte System

1. Make the following change on the Dynabyte CPU board:

   Lift pin 11 of IC 12C (4th IC in from the right on bottom row, 74LS373) from its socket.

2. Configure the 1st 64K of memory as follows for a single user system or as the first board of an MP/M system using 32K memory banks.

   A. Set switches S1 - S5 as follows:

S1 S2 S3 S4 S5

   B. Wire Header No. 2 as Follows:

      pin 1 to pins 15 and 17
      pin 2 to pins 11 and 13

   C. Wire Header No. 1 the same as the Cromemco Z80 as shown in Table 2, sheet 10.

   D. Wire the 2 pads in jumper area B together. This connects a pull up resistor to PHANTOM.

3. Set up additional 64K memory boards as two 32K memory banks for MP/M as follows:

   A. Set switches S1 - S5 as follows:

S1 S2 S3 S4 S5

   B. Wire Header No. 2 as follows

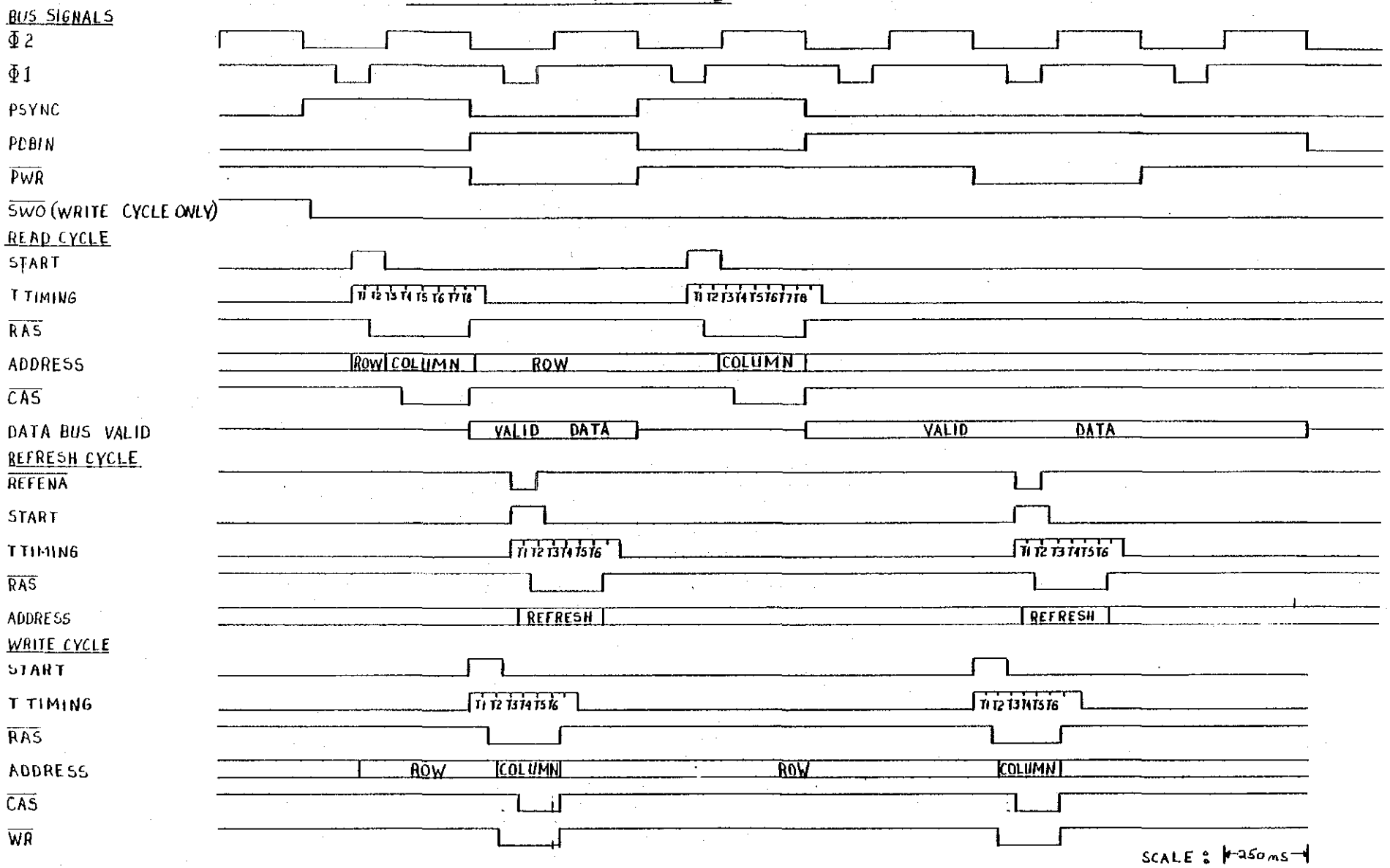
      pin 3 to pins 15 and 17 — Board 2
      pin 4 to pins 11 and 13

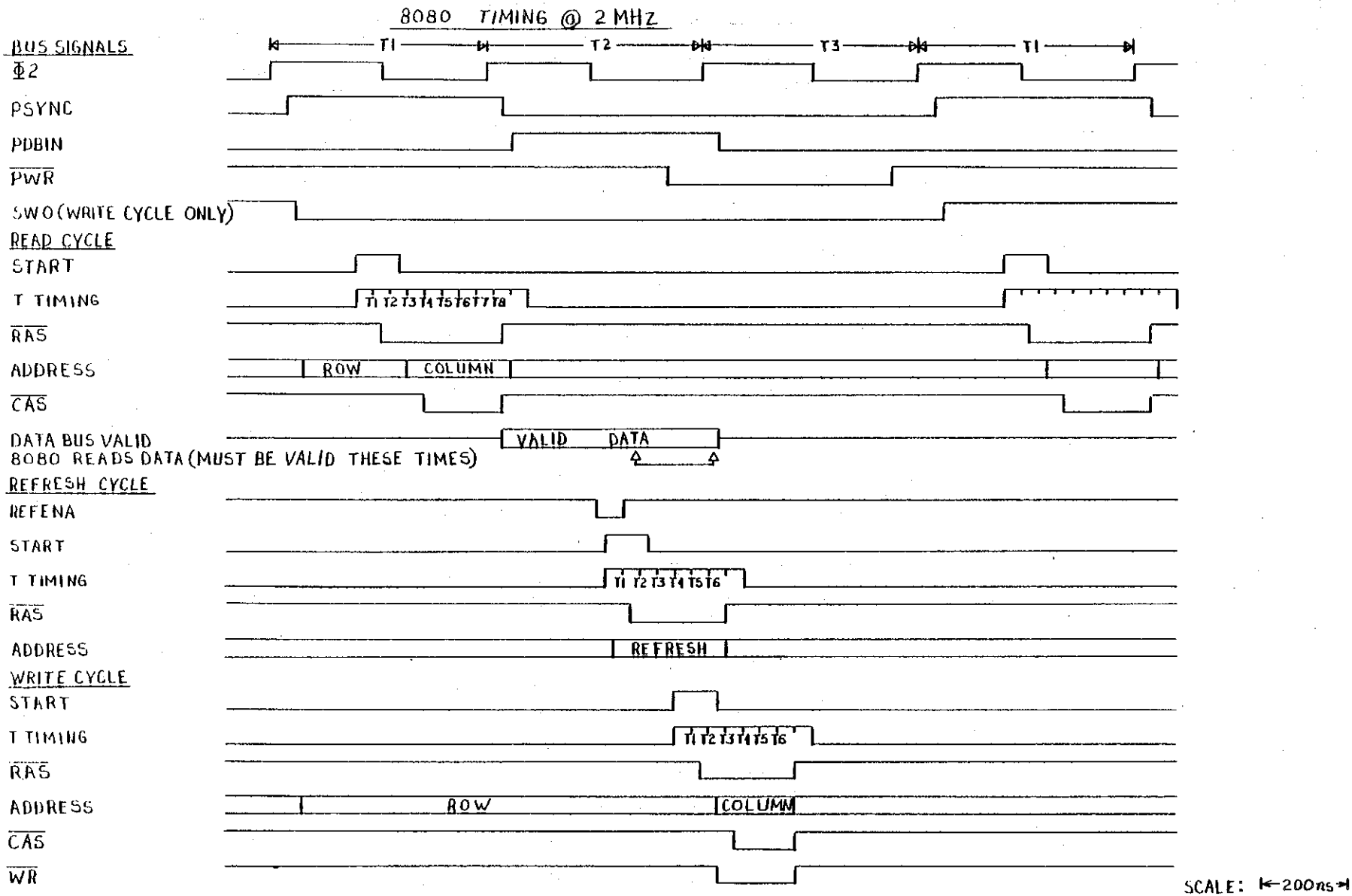
      pin 5 to pins 15 and 17 — Board 3
      pin 6 to pins 11 and 13

      pin 7 to pins 15 and 17 — Board 4
      pin 8 to pins 11 and 13

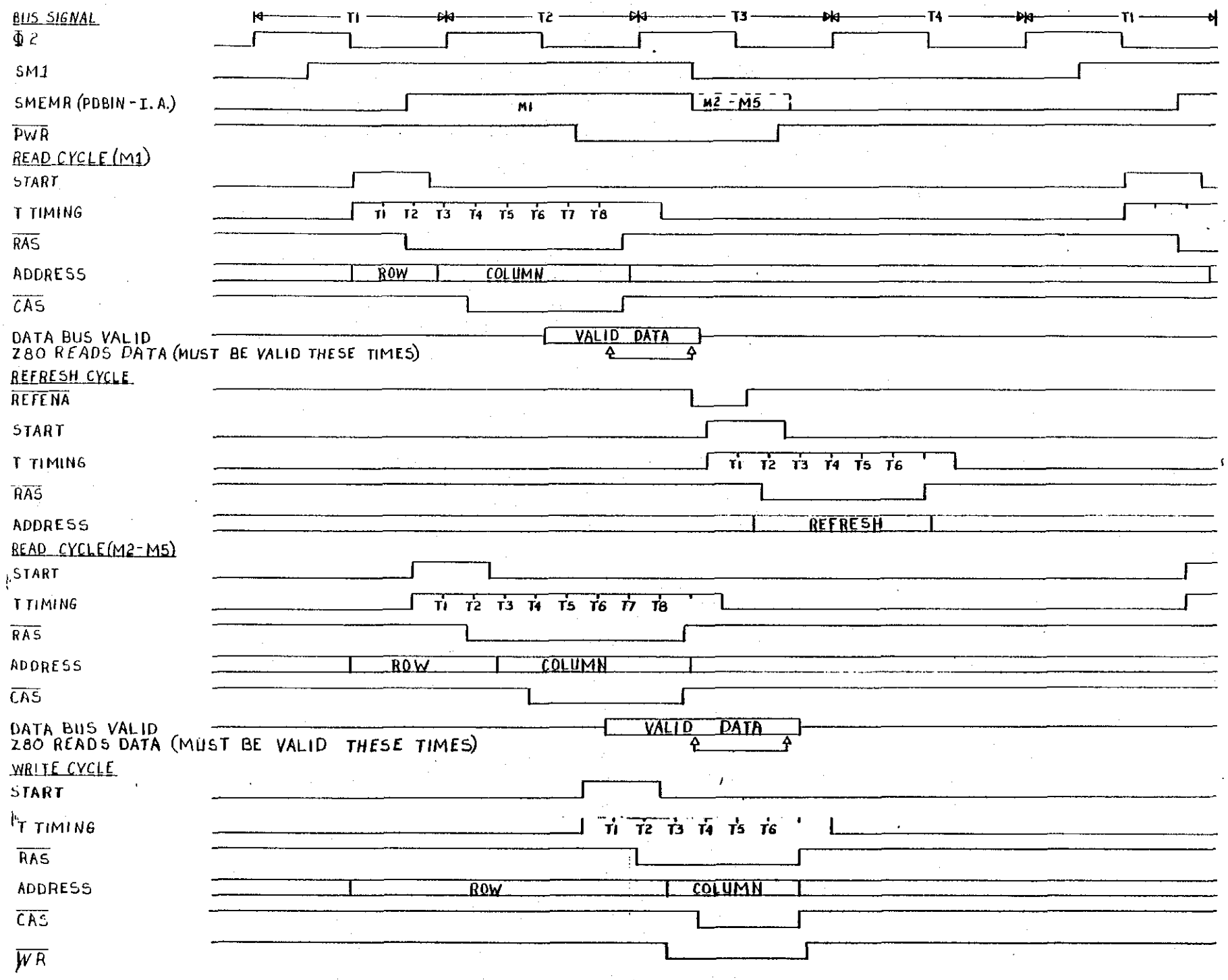
   C. Wire Header No. 1 to the same as board 1.

ALPHA MICRO TIMING @ 2 MHz




8080 TIMING @ 2 MHz
BUS SIGNALS
T1
T2
T3
T1
Φ2
PSYNC
PDBIN
PWR
SWO (WRITE CYCLE ONLY)
READ CYCLE
START
T TIMING
T1 T2 T3 T4 T5 T6 T7 T8
RAS
ADDRESS
ROW
COLUMN
CAS
DATA BUS VALID
VALID DATA
8080 READS DATA (MUST BE VALID THESE TIMES)
REFRESH CYCLE
REFENA
START
T TIMING
T1 T2 T3 T4 T5 T6
RAS
ADDRESS
REFRESH
WRITE CYCLE
START
T TIMING
T1 T2 T3 T4 T5 T6
RAS
ADDRESS
ROW
COLUMN
CAS
WR
SCALE: ⟵200ns⟶

Z80 TIMING @ 4 MHz - CROMEMCO, NORTHSTAR, ITHACA AUDIO, VECTOR GRAPHIC, ETC.



SCALE: ⟵100ns⟶

Z80 TIMING @ 2 MHz - CROMEMCO, NORTH STAR, ITHACA AUDIO, VECTOR GRAPHIC, ETC.